data, respectively, and wherein the video graphics display further comprises a controller operably coupled to the video scaler and the graphics scaler, wherein the controller provides control information to the video scaler and the graphics scaler, wherein scaling operations of the video scaler and the graphics scaler utilize the control information.

4. (Amended) A video graphics display engine comprising:

a video scaler adapted to receive a video data stream in a first format, wherein the video scaler scales video images in the video data stream based on a ratio between the video images in the first format and an output video image to produce a scaled video stream;

a graphics scaler adapted to receive a graphics data stream in a second format, wherein the graphics scaler scales graphics images in the graphics data stream based on a ratio between the graphics images in the second format and an output graphics image to produce a scaled graphics stream;

a merging block operably coupled to the video scaler and the graphics scaler, wherein the merging block combines the scaled video stream and the scaled graphics stream to produce a video graphics output stream; and

a single memory operably coupled to the graphics scaler and to the video scaler, the single memory further comprises a first memory block and a second memory block, wherein the stream of video data is fetched from the first memory block and the stream of graphics data is fetched from the second memory block.

5. (Amended) The display engine of claim 4, wherein the single memory is included in a frame buffer of a video graphics integrated circuit.

6. (Amended) The display engine of claim 4, wherein the controller further comprises a video controller operably coupled to a graphics controller,

wherein the video controller is operably coupled to the video scaler, wherein the video controller provides a first portion of the control information to the video scaler, wherein the graphics controller is operably coupled to the graphics scaler, wherein the graphics controller provides a second portion of the control information to the

graphics scaler, and

wherein the video controller and the graphics controller are synchronized.

7. (Amended) The display engine of claim 4, wherein the merging block performs an alpha blend operation on the scaled video stream and the scaled graphics stream to produce the video graphics output stream.

8. (Amended) The display engine of claim 4 further comprises a digital to analog converter operably coupled to the merging block, wherein the digital to analog converter converts the video graphics output stream to an analog display signal.

9. (Amended) The display engine of claim 4 further comprises a display driver operably coupled to the merging block, wherein the display driver is adapted to receive the video graphics output stream in digital format, wherein the display driver formats the video graphics output stream in a display compatible format.

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10. (Amended) The display engine of claim 4 further comprises a display driver operably coupled to the video scaler, wherein the display driver is adapted to receive the scaled video stream and produce a video display output based on the scaled video stream.

11. (Amended) The display engine of claim 4 further comprises a display driver operably coupled to the graphics scaler, wherein the display driver is adapted to receive the scaled graphics stream and produce a graphics display output based on the scaled graphics stream.

12. (Amended) The display engine of claim 4 further comprises a graphics flicker removal block operably coupled to the graphics scaler, wherein the graphics flicker removal block removes flicker from the scaled graphics stream.

13. (Amended) The display engine of claim 4 further comprises a video flicker removal block operably coupled to the video scaler, wherein the video flicker removal block removes flicker from the scaled video stream.

14. (Amended) The display engine of claim 4 further comprises a plurality of graphics scalers, wherein each of the plurality of graphics scalers receives the graphics data stream and scales the graphics images in the graphics data stream based on a ratio between the graphics images in the second format and a corresponding output graphics image to produce a corresponding scaled graphics stream.

15. (Amended) The display engine of claim 4, wherein the merging block further comprises circuitry which configures a pixel rate of the video graphics output stream to produce a preferred video scaling ratio, wherein the preferred video scaling ratio is based on the ratio between the video images in the first format and the output video image.

16. (Amended) The display engine of claim 4, wherein the merging block further comprises circuitry which configures a pixel rate of the video graphics output stream to produce a preferred graphics scaling ratio, wherein the preferred graphics scaling ratio is based on the ratio between the graphics images in the second format and the output graphics image.

17. (Amended) The display engine of claim 4 further comprises a video decompression block operably coupled to the video scaler, wherein the video decompression block receives a compressed stream of video data and decompresses the compressed stream of video data to produce the video data stream.

18 (Amended) The display engine of claim 4 further comprises a graphics decompression block operably coupled to the graphics scaler, wherein the graphics decompression block receives a compressed stream of graphics data and decompresses the compressed stream of graphics data to produce the graphics data stream.

19. (Amended) The display engine of claim 4, wherein the video data stream is a decoded MPEG data stream.

20. (Amended) A method for displaying video graphics data comprising:

receiving a video data stream, wherein the video data stream includes video data in a first format;

allocating a first block of a memory for storing the video data stream, the allocating based upon memory needs of the video data stream;

receiving a graphics data stream, wherein the graphics data stream of includes graphics data in a second format;

allocating a second block of the memory for storing the graphics data stream, the allocating based upon memory needs of the graphics data stream;

scaling the video data based on a ratio between the first format and a selected video format to produce a scaled video stream;

scaling the graphics data based on a ratio between the second format and a selected graphics format to produce a scaled graphics stream; and

merging the scaled video stream and the scaled graphics stream to produce a video graphics output stream.

30. (Amended) A video graphics integrated circuit comprising:

a frame buffer having memory, wherein the video graphics integrated circuit allocates memory between video data and graphics data based upon memory needs of the video data and the graphics data;

a video scaler operably coupled to the frame buffer, wherein the video scaler scales the video data to produce a scaled video data stream;

a graphics scaler operably coupled to the frame buffer wherein the graphics scaler scales the graphics data to produce a scaled graphics data stream; and

a merging block operably coupled to the video scaler and the graphics scaler, wherein the merging block combines the scaled video data stream and the graphics data stream to produce a video graphics output stream.

31. (Amended) A video graphics circuit comprising:

a plurality of memory blocks, wherein each of the plurality of memory blocks stores at least one of video data and graphics data;

a plurality of video scalers, wherein each of the plurality of video scalers is coupled to at least one of the plurality of memory blocks, wherein each video scaler of the plurality of video scalers independently scales at least a portion of the video data to produce a scaled video data stream of a plurality of scaled video data streams independent from the other scaled video data streams of the plurality of scaled video data streams;

a plurality of graphics scalers, wherein each of the plurality of graphics scalers is coupled to at least one of the plurality of memory blocks, wherein each graphics scaler of the plurality of graphics scalers independently scales at least a portion of the graphics data to produce a scaled graphics data stream of a plurality of scaled graphics data streams independent from the other scaled graphics data streams of the plurality of scaled graphics data streams; and

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a plurality of merging blocks, wherein each of the merging blocks is operably coupled to at least one video scaler of the plurality of video scalers and at least one graphics scaler of the plurality of graphics scalers such that each of the merging blocks receives a plurality of scaled data streams, wherein each merging block combines received scaled data streams to produce a video graphics output stream of a plurality of video graphics streams.

34. (Amended) The video graphics circuit of claim 31 further comprises a plurality of controllers, wherein each of the plurality of controllers is operably coupled to at least one scaler of a combined set of scalers that includes the plurality of graphics scalers and the plurality of video scalers, wherein each of the plurality of controllers provides separate control information that controls independent scaling by scalers to which it is coupled.

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REMARKS

Reconsideration of the rejection of claim 6 under 35 U.S.C. §112 because of insufficient antecedent basis is respectfully requested in light of the modification to claim 6. By this amendment, the limitation "the data controller", in line 8, has been replaced with the limitation "the graphics controller". The dependency of claim 6 was also changed.